NORMAL SIGNAL TRACING

UNCLASSIFIED

CF351L08-01

RISK ASSESSMENT: *Low*

SAFETY CONSIDERATIONS:

Electrical Shock Hazard

Electrostatic Discharge

ENVIRONMENTAL CONSIDERATIONS:

None

TERMINAL LEARNING OBJECTIVE

ACTION: Identify normal signal conditions of the microprocessor.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA electronic trainer, logic probe, and official OMEMS reference material.

STANDARDS: Measure and record the normal signal conditions of the microprocessor without error.

ENABLING LEARNING OBJECTIVE

ACTION: Explain the normal signal tracing matri

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA electronic trainer, and official OMEMS reference material.

STANDARDS: Utilize the matrix to identify the correct source and destination of the microprocessor signals.

IC NAME

SIGNAL NAME

PIN NUMBER

ORIGIN

DESTINATION

PURPOSE

CONDITION (H/L/P)

CONDITION DURING RESET

CF351L08-05

ENABLING LEARNING OBJECTIVE

ACTION: Measure and record the signals of the Nida 500 microprocessor.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA electronic trainer, logic probe, and official OMEMS reference material.

STANDARDS: Measure and record the signals of the microprocessor while understanding the purpose of the signal and the role in which it plays in the microprocessor system.

MEASURE AND RECORD SIGNALS OF THE U2 CLOCK GENERATOR

CF351L08-07

U2 Clock Generator:

IC Name	Signal Name	Pin Number	Origin Dest	Purpose
U2 Clock Generator	Ready	5	U2/5	U1/22 wait state
	CLK	8	U2/8	U1/19 CPU clk
	Reset	10	U2/10	U1/21 reset
	RES	11	SW1	

MEASURE AND RECORD SIGNALS OF THE U1 CPU

CF351L08-09

U1 CPU processor:

IC Name	Signal Name	Pin Number	Origin Dest	Purpose
U1 CPU	Ready	22	U2/5 U1/22	wait state
	CLK	19	U2/8 U1/19	CPU clk
	Reset	21	U2/10 U1/21	reset
	IO/M	28	U1/28 U38/1	sel IO/M
	RD	32	U1/32	

U1 CPU continued:

IC Name	Signal Name	Pin Number	Origin	Dest	Purpose
U1 CPU	Bufer/ Bi-direction	27	U1/27	U9-U11	
1	Buff enable W			pin	
	Buffen	26	U1/26	U4/7	Enable Aen
					Ben, Cen
	ACTR	25	U1/25	U6	

MEASURE AND RECORD SIGNALS OF THE U4 DECODER

U4 Decoder chip:

IC Name	Signal Name	Pin Number	Origin Dest	Purpose
U4	IO/M	1	U38/3	
U4/1	sel IO/M			
Decoder				
	RD	2	U1/32	
U4/2	RD IO/M			
	WR	3	U1/29	
U4/3	WR IO/M			
	A0	4	U6/19	
U4/4	Addr Lsb			

U4 Decoder continued:

IC Name	Signal Name	Pin #	Origin	Dest	Purpose
U4 Decoder	MEMRD	12	U4/12	U12-U15	RD mem pin 22
	MWRHI	19	U4/19	U15/27	RAM HI
	MWLO	13	U4/13	U14/27	RAM LO
	IORD	14	U4/14		

U4 Decoder continued:

IC Name	Signal Name	Pin Number	Origin	Dest	Purpose
U4	AEN	16	U4/16	U9/19	Buff LO Decoder enable
	BEN	17	U4/17	U11/19	Buff HI enable
	GEN	18	U4/18		

MEASURE AND RECORD SIGNALS OF THE U6-U8 ADDRESS LATCHES

C

OC

CF351L08-

U6-U8 Address Latches:

IC Name	Signal Name	Pin #	Origin	Dest Pin
U6-U8 Addr 11 Latches	C strobe	11	U1/25	U6-U8 Addr pin
GND	OC Addr latch	1	GND	

MEASURE AND RECORD SIGNALS OF THE U9,U11 DATA BUFFERS

G

DIR

CF351L08-

U9 and U11 Data Buffers:

IC Name	Signal Name	Pin #	Origin	Dest Pin
U9, U11 Buff Data 19 Byte Buffers Enable	G	19	U4/16,17	U9-U11
	DIR	1	U1/27	U9-U11

MEASURE AND RECORD SIGNALS OF THE U12,U13 ROM

CE

OE

CF351L08-

U12 and U13 ROM chips:

IC Name	Signal Name	Pin #	Origin	Dest Purpose
U12, U13 ROM	CE	20	U16B/8	U12, U13 Sel ROM pin 20
	OE	22	U4/12	U12, U13 RD ROM

MEASURE AND RECORD SIGNALS OF THE U14,U15 RAM

CS

OE

WE

U14 and U15 RAM chips:

IC Name	Signal Name	Pin #	Origin	Dest Purpose
U14, U15 RAM	CS Sel	20	U16A/6	U14, U15 RAM pin 20
U14, U15 RAM	OE RD	22	U4/12	U14, U15 RAM pin 22
	WE	27	U4/13	

SUMMARY

MEASURE SIGNALS ON THE NIDA 500 TRAINER.

WILL HELP ISOLATE THE FAULT

CONSIDER WHAT THE SIGNAL IS USE FOR